IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

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1. (Amended) An overlay target comprising:
at least one trench having a bottom surface, said one trench including a series of substantially vertically extending raised lines originating at said bottom surface of said trench.

2. The overlay target of claim 1, wherein said at least one trench comprises a continuous trench defining a geometric shape.

3. (Amended) The overlay target of claim 1, wherein said at least one trench comprises a plurality of trenches defining said overlay target, each of said plurality of trenches includes said series of substantially vertically extending raised lines originating at said bottom surface of said trench.

4. The overlay target of claim 3, wherein said plurality of trenches includes at least one continuous trench defining a geometric shape.

5. (Amended) An overlay target comprising:
at least one pad area having a bottom surface, said one pad area including a series of substantially vertically extending raised lines originating at said bottom surface of said pad area.

6. (Amended) The overlay target of claim 5, wherein said at least one pad area includes a plurality of pad areas defining said overlay target, each of said plurality of pad areas

includes said series of substantially vertically extending raised lines originating at said bottom surface of said pad area.

7. (Amended) The overlay target of claim 6, further comprising at least one trench including said series of substantially vertically extending raised lines originating at said bottom surface of said overlay target.

8. (Amended) A semiconductor wafer comprising:
a semiconductor substrate; and
an overlay target having a bottom surface comprising at least one series of substantially vertically extending raised lines originating at said bottom surface of said overlay target.

9. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is etched into said semiconductor substrate.

10. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is etched into a material layer overlying said semiconductor substrate.

11. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is disposed in at least one trench.

12. (Amended) The semiconductor wafer of claim 11, wherein a plurality of trenches and a corresponding plurality of series of substantially vertically extending raised lines define said overlay target, each of said plurality of trenches includes one of said plurality of series of substantially vertically extending raised lines.

13. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is disposed in at least one pad area.

14. (Amended) The semiconductor wafer of claim 13, wherein a plurality of pad areas and a corresponding plurality of series of substantially vertically extending raised lines define said overlay target, each of said plurality of pad areas includes one of said plurality of series of substantially vertically extending raised lines.

15. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines comprises a first series of raised lines disposed in a pad area and a second series of raised lines disposed in a trench.